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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/904,951 | 07/13/2001 | Wolfram Kluge | 2000.066200/DE0029 | 4131 |

23720 7590 10/21/2004

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| EXAMINER | |
|---|---|
| JACKSON, BLANE J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2685 | |

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/904,951 | KLUGE ET AL. | |
| | Examiner | Art Unit | |
| | Blane J Jackson | 2685 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durec (U.S. Patent 6,144,846) with a view to Razavi et al. (U.S. Patent 6,748,204).

As to claims 1 and 12-14, Durec teaches a mixer comprising:

A multiplier circuit having a first and a second mixer (figures 1-4, first mixer (14A), second mixer (14B),

A generator for generating two first and two second control signals for controlling the first and second mixers (figure 2, Vosc (26), counters (28x) and phase shifters (30x)),

wherein the two first control signals have a frequency f1 and two second control signal have a frequency of f2 (figure 1, frequency f2 adjusted by Nsel to counter (28), column 9, lines 7-26).

Durec teaches a compound mixer in a differential configuration comprising a first and second four transistor Gilbert type mixer cores current sourced by a transconductance stage (figure 4, (58) of two transistors where the transconductance stage provides a differential input for the RF frequency to be mixed and current bias control (figure 4, column 6, line 5 to column 7, line 33). Durec does not teach the first mixer comprising a first number of transistors and the second mixer comprising a second number of transistors, the first number being different than the second number.

Razavi teaches a contemporary mixer circuit for combining an RF signal and a differential local oscillator signal to provide a differential frequency conversion output that is comprised of a pair of transistors and bias circuits (figure 1, column 1, lines 21-45). It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute the transconductance circuit of Durec for the differential mixer circuit of Razavi as an alternative configuration to simplify but provide a compound mixer without the bias power loss of an additional Gilbert mixer core.

As to claims 2 and 3 Durec teaches the two first and two second control signals are balanced (differential) or single ended signals (figures 3 and 4, column 5, line 59 to column 6, line 4).

4. Claims 4-11 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bojer (U.S. Patent 6,029,059) with a view to Razavi et al. (U.S. Patent 6,748,204) and Durec (U.S. Patent 6,144,846).

As to claims 4, 6-8 and 15-18, Bojer teaches a mixer for I/Q quadrature signal generation comprising:

A first multiplier circuit having a (second) mixer (figure 3, four transistors T5-T8 configured as a Gilbert cell (60)),

A second multiplier circuit having a (fourth) mixer (figure 3, four transistors T9-T12, Gilbert cell (62), column 4, lines 8-17),

A generator for generating two control signals for controlling the mixers,

Wherein the two control signals are in each case balanced signals of frequency F2,

frequency F2 is provided in four phases each shifted by 180 degrees (LO provided in four phases, in balanced, 180 degree input, I+ and I- to the (second) mixer and Q+ and Q- to the (fourth) mixer, a dual balanced quadrature mixer, column 3, line 64 to column 4, line 62).

Bojer teaches a single stage (second and fourth mixers) quadrature mixer but does not teach a (first, second, third and fourth) two stage quadrature compound mixer where the two (first and third mixer of the first stage) control signals are balanced, provided in four phases and have a different frequency F1.

Bojer also teaches a pair of transconductance circuits comprised of a pair of transistors to input a balanced input signal (RF) and bias control to each provide a differential output to input a respective mixer core (figure 3, transistor pairs T1-T2 and T3-T4, column 3, line 66 to column 4, line 10).

Razavi teaches a contemporary balanced mixer circuit for combining an RF signal and a differential local oscillator signal to provide a differential frequency conversion output that is comprised of a pair of transistors and bias circuits (figure 1, column 1, lines 21-45). It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute the transconductance circuit of Bojer for the differential mixer circuit of Razavi to provide a two stage balanced quadrature mixer circuit without additional circuit stages and power loss.

The combination of Bojer and Razavi do not teach a generator for generating two first and two second control signals for controlling the first and second mixers and two third and two fourth control signals for controlling the third and fourth mixers of the two stage quadrature mixer.

Durec teaches a compound differential mixer (not quadrature) with a generator for generating two first and two second control signals for controlling the first and second mixers where the fist and second signals are case balanced signals of different frequencies F1 and F2 that differ from an operation frequency of the generator using frequency division to derive the different frequencies. Durec teaches the frequency translation circuit configured for single ended or differential outputs (figure 3, frequency translation circuit (40), Vosc (26), counters (28x) and phase shifters (30x), column 5, line 59 to column 6, line 4).

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the system of Bojer and Razavi with the multiple balanced output generator of Durec to drive the Gilbert cell mixers.

As to claim 5, Bojer teaches the mixer of claim 4 wherein the first and second multiplier circuits each comprise a Gilbert cell having a plurality of transistors where all transistors are used as switches (figure 3, mixer transistor group (T5-T8) and mixer transistor group (T9-T12) depict conventionally known Gilbert cell architecture of a three port a mixer core comprised of transistors to receive an input (RF) signal and are switched at the rate of the applied balanced oscillator to output an intermediate frequency signal, column 4, lines 8-10).

As to claim 9, Durec of Bojer modified does not teach that the frequency derivation circuit is executed by using frequency multiplication. However, it is well known in the art several schemes to derive a local oscillator frequency for frequency conversion circuits including a voltage controlled oscillator, harmonic amplifiers (multipliers) and, as discussed by Durec, divide by methods. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to recognize in the frequency derivation methods of Durec modified other methods to generate an LO frequency.

As to claims 10 and 11, Bojer modified teaches a double balanced quadrature mixer that inherently suppresses LO leakage and products comprised of the local oscillators thereby voltages or currents within the circuit avoid the sum frequency of F1+F2 and the difference frequency F1-F2.

***Conclusion***

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Blane J Jackson whose telephone number is (703) 305-5291. The examiner can normally be reached on Monday through Friday, 8:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (703) 305-4385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BJJ

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